NON-VOLATILE SEMICONDUCTOR MEMORY DEVICE

TP This application is a division of SN 10/006,395, filed on 12/9/2001, which is now U.S. Patent No. 6,639,837.

CROSS-REFERENCE TO RELATED APPLICATION

This application is based on and claims the benefit of priority from the prior Japanese Patent Application No. 2000-376501, filed on December 11, 2000, the entire contents of which are incorporated herein by reference.

BACKGROUND OF THE INVENTION

Field of the Invention

This invention relates to non-volatile electrically rewritable or "reprogrammable" semiconductor memory devices. More particularly, but not exclusively, the invention relates to electrically erasable and programmable read only memory devices.

Description of the Related Art

Electrically erasable programmable read only memories (EEPROMs) are arranged to include an array of memory cells, each of which typically has a transistor structure with a floating gate for electrical carrier retention and a control gate as insulatively stacked or "multilayered" over the floating gate. This memory cell is designed to exhibit a threshold voltage-increased state with electrons injected into the floating gate and a threshold voltage-decreased state with the floating gate electrons released away, which are used for storage of binary digital data bits of a logic "1" and a "0," respectively. The memory cell's data may be read out by first giving a read voltage to the control gate thereof and then detecting or sensing whether this cell